IN THE CLAIMS

The following are Claims 1-21, with Claims 2, 3, 12, 13, 18, and 19 canceled.

1. (currently amended) A circuit comprising:

a comparator adapted to receive a first and a second input signal and provide a comparator output signal;

a first register adapted to store at least one threshold value and at least one successive approximation register value;

a digital-to-analog converter adapted to provide the second input signal to the comparator, where the second input signal is based on one of the threshold values or one of the successive approximation register values from the first register; ~~and~~

a first multiplexer adapted to select from one or more input signals to provide a first output signal;

a sample and hold circuit adapted to store a value of the first output signal and provide a second output signal; and

a second multiplexer adapted to select between the first and second output signal to provide the first input signal to the comparator; and

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a second register adapted to store the comparator output signal from the comparator, wherein the circuit is adapted to provide threshold detection or successive approximation analog-to-digital conversion of the first input signal.

2. (canceled)

3. (canceled)

4. (currently amended) The circuit of Claim 1, further comprising cycling logic adapted to control the first and second multiplexers to select the first input signal, from among a number of input signals, to provide to the comparator.

5. (original) The circuit of Claim 4, wherein the cycling logic is further adapted to select the threshold value or the successive approximation register value to provide as the second input signal to the comparator.

6. (original) The circuit of Claim 4, wherein the cycling logic is further adapted to select a location in the second register to store the comparator output signal.

7. (original) The circuit of Claim 1, further comprising successive approximation register logic adapted to control a value for the at least one successive approximation register value based on the comparator output signal.

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8. (original) The circuit of Claim 1, wherein the comparator output signals stored in the second register provide the results from threshold detection operations of the comparator.

9. (original) The circuit of Claim 1, wherein the successive approximation register value is a result of an analog-to-digital conversion upon completion of a successive approximation analog-to-digital conversion operation by the circuit.

10. (original) The circuit of Claim 1, wherein the first register comprises a register bank of at least two registers, with one register adapted to store at least a threshold value and the other register adapted to store at least a successive approximation register value.

11. (currently amended) A circuit comprising:

a comparator adapted to receive a first and a second input signal and provide a comparator output signal;

means for providing the first input signal to the comparator, wherein providing includes selecting one from among a number of input signals to provide as the first input signal, with at least one of the input signals being selectively sampled and held and selectively provided as the first input signal; and

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means for storing and selecting one from a number of threshold values and one or more successive approximation register values to generate the second input signal to the comparator.

12. (canceled)

13. (canceled)

14. (original) The circuit of Claim 11, further comprising means for storing comparator output signals to provide as comparison results.

15. (original) The circuit of Claim 11, further comprising means for updating one of the successive approximation register values based on the comparator output signal to provide successive approximation analog-to-digital conversion.

16. (original) The circuit of Claim 11, further comprising means for cycling through the input signals to provide comparator results and/or successive approximation analog-to-digital conversion.

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17. (currently amended) A method of providing analog-to-digital conversion and threshold detection, the method comprising:

receiving a number of input signals, wherein at least one of the input signals is selectively sampled and stored;

providing a first input signal selected from the input signals, including the at least one sampled and stored input signal;

selecting a threshold value or a successive approximation register value to convert and provide as a second input signal;

comparing the first input signal to the second input signal to provide a comparator output signal;

providing the comparator output signal as a threshold detector result if one of the threshold values was selected; and

providing the comparator output signal as a comparison result for successive approximation analog-to-digital conversion if the successive approximation register value was selected.

18. (canceled)

19. (canceled)

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20. (original) The method of Claim 17, wherein the comparison result is used to update the successive approximation register value for successive approximation analog-to-digital conversion.

21. (original) The method of Claim 17, further comprising storing the threshold detector results and providing as threshold comparison output signals.

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